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## Naim Digital to Analogue Converter

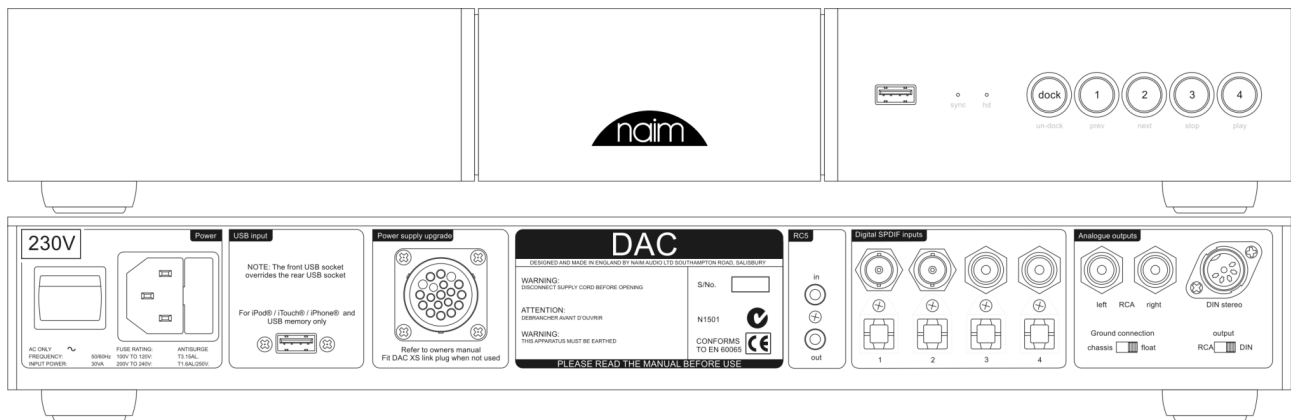
Design, Engineering & Technology

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### Objective

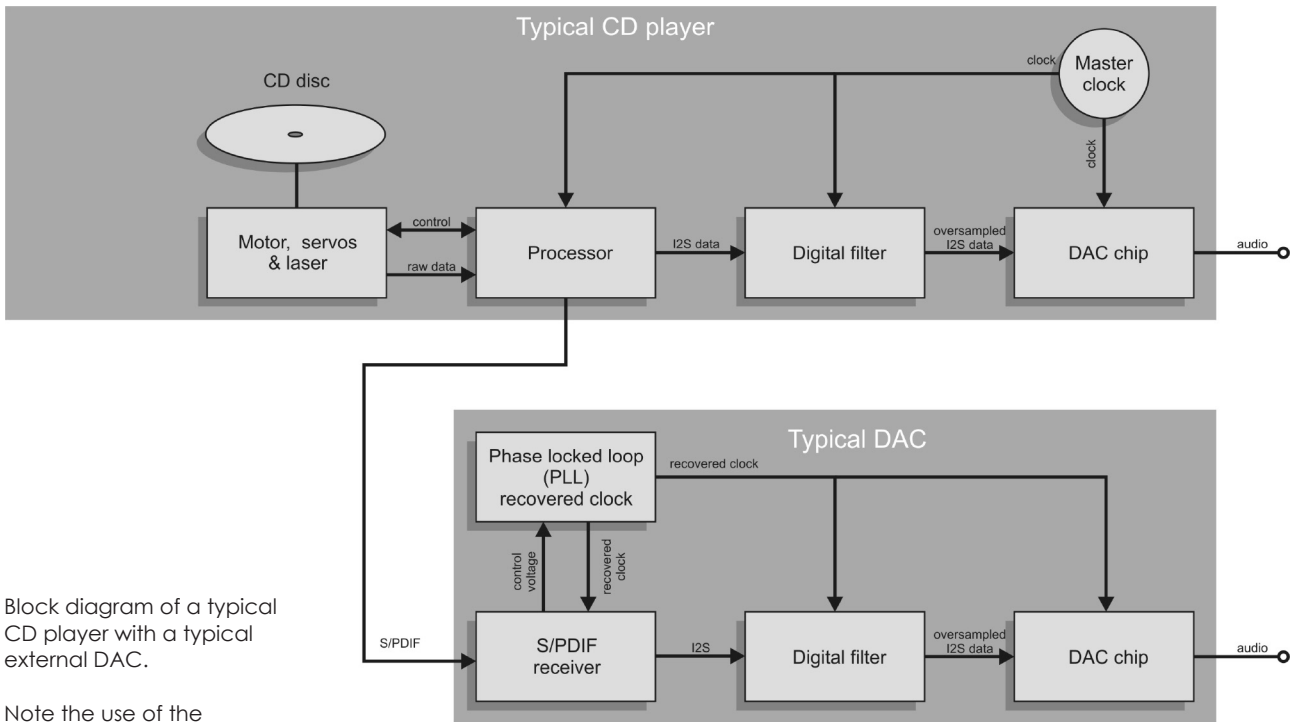
To design a standalone digital to analogue converter that is sonically comparable to a high-end CD player.



### Overview

Since 1991 when the first Naim CD player – the CDS – was launched, Naim's design philosophy has been that for best sonic performance from digital audio the master clock must be positioned close to the DAC chips. When the clock and DAC chips are closely coupled, timing errors are minimised. Whereas if a CD player is connected to an external DAC via S/PDIF, the master clock is in the CD player and the DAC chips are in the DAC, ie they

are separated by the S/PDIF interface. The DAC has to recover the clock from the S/PDIF signal, and this can easily introduce timing errors (jitter). Moreover, S/PDIF circuitry represents a radio frequency (RF) noise source and its presence in a CD player is audible. Consequently, Naim has never fitted S/PDIF outputs to its CD players and has never developed an external DAC – until now.



Block diagram of a typical CD player with a typical external DAC.

Note the use of the recovered clock to control the DAC chips

Given these technical obstacles, why has Naim designed an external DAC?

When CD was the primary source of high quality digital audio there was no motivation to engineer an external DAC: it was better to continue the integrated CD player model since it would always be superior on a performance/cost basis. But the nature of audio delivery is changing. As the price of digital storage falls by approximately half each year, so effectively limitless hard disk storage of CD-quality and high-resolution audio becomes a realistic prospect. Today audio is increasingly played back from computers, streaming network players and hard disk players such as the Naim HDX. Modern televisions, games consoles and portable audio players are also digital. An external DAC capable of the same sound quality as a high-end CD player would significantly upgrade all these devices.

How to overcome the problem of S/PDIF induced jitter

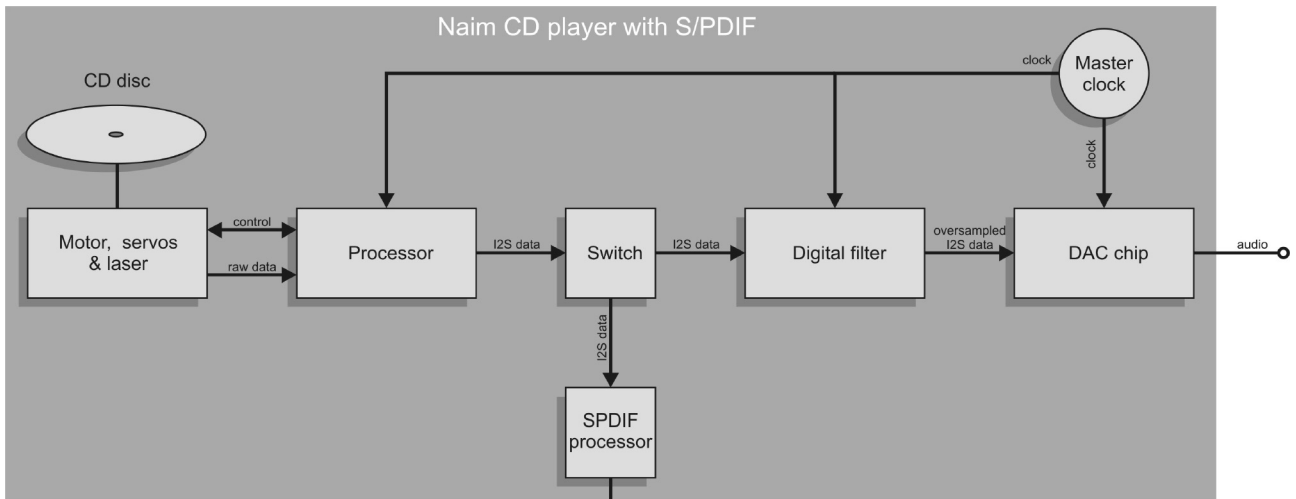
In the Naim DAC the master clock is not recovered from the S/PDIF signal as usual. Instead the audio data is read from S/PDIF, stored in solid-state memory and then clocked back out to the DAC chips using a fixed-frequency local master clock. This eliminates jitter caused by S/PDIF. In essence the memory, master clock and DAC structure behaves in a similar manner to the CD, master clock and DAC structure of a CD player.

How to overcome the problem of adding S/PDIF circuitry to a high-end CD player

Naim's new CD5 XS and CDX2-2 are both fitted with S/PDIF output. At the heart of these players is a Philips SAA7324 digital servo processor running Naim custom controller software. This chip controls the disc mechanism and includes an integrated S/PDIF generator but our research has shown that sound quality is compromised if the SAA7324's S/PDIF generator is used. So in the CD5 XS and CDX2-2 the S/PDIF signal is generated instead by a dedicated processor that can be turned off when the digital output is not in use. In this way S/PDIF output is prevented from affecting sound quality when the analogue output is being used.

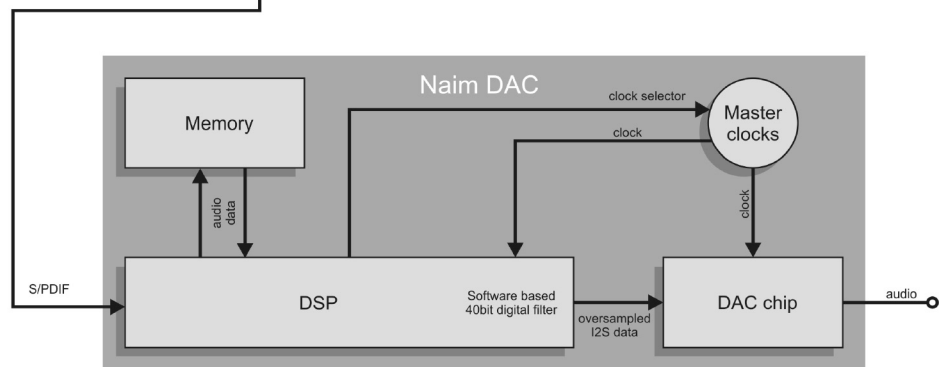
How to overcome the problem of S/PDIF noise entering a DAC

The Naim DAC's high-speed DSP (digital signal processor) front-end is electrically isolated from its high-resolution DAC and analogue circuits. Also, the two sections are run from separate power supplies. Together these measures significantly reduce the digital RF noise which could affect the analogue stage.



Block diagram of a Naim S/PDIF-enabled CD player with the Naim DAC. Note in the CD player that the S/PDIF circuitry can be turned off when not in use.

In the external DAC, the DAC chips are controlled by a master clock, similarly to the CD player



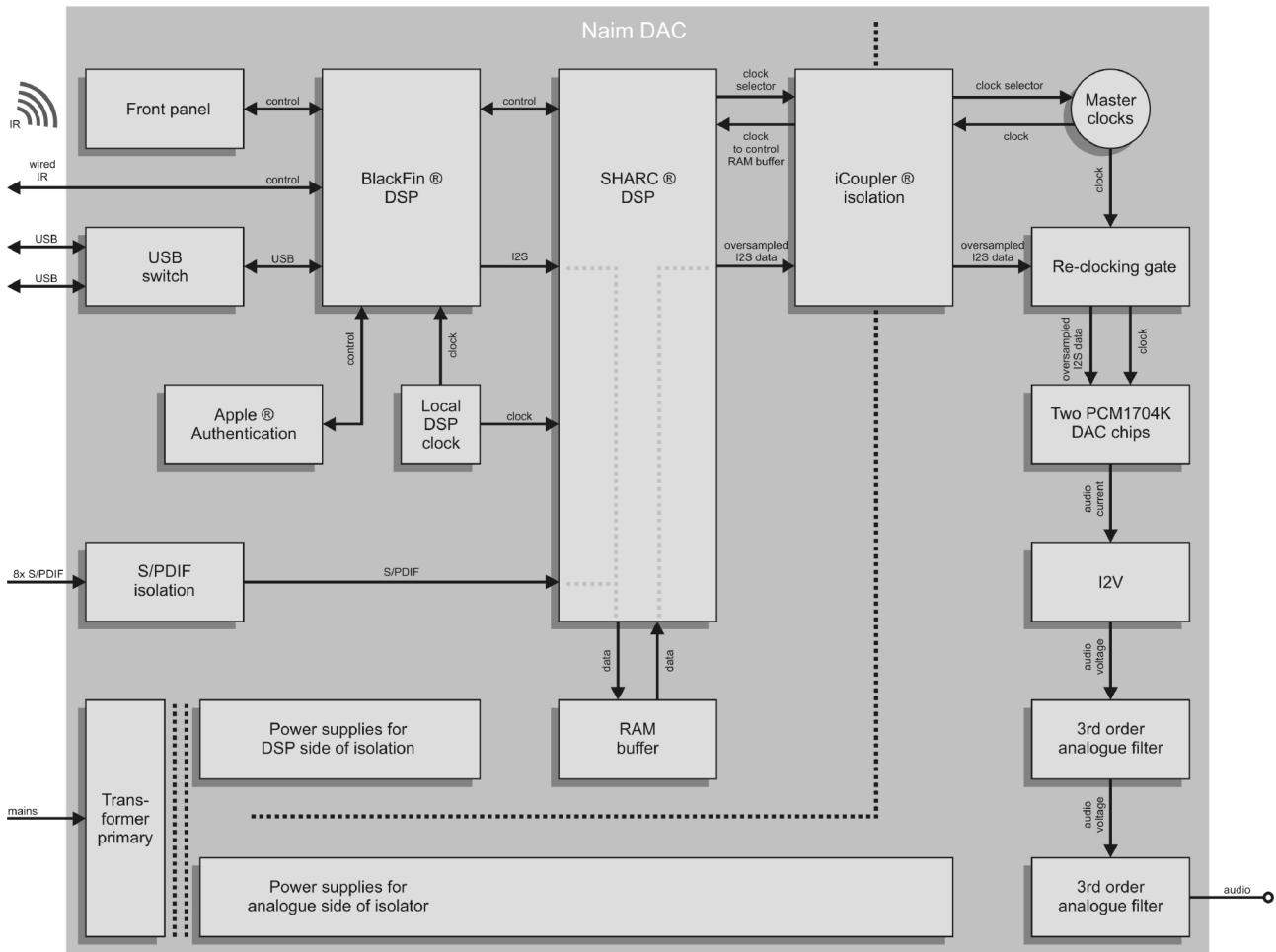
### S/PDIF and I<sup>2</sup>S

S/PDIF (which has now been incorporated into the expanded AES3 digital interface specification) is the industry standard for real-time transfer of digital audio from one consumer audio product to another. Within a product the same digital audio signal is transferred between devices via a different interface called I<sup>2</sup>S (also known as I<sup>2</sup>S or IIS). I<sup>2</sup>S uses three separate connections – audio data, word clock and bit clock – whereas S/PDIF combines all three signals into one using bi-phase coding. As a result, when S/PDIF is decoded inside an external DAC the data, word clock and bit clock have to be separated. But when the clock is recovered its frequency can be modulated by the digital data, resulting in data-related jitter. Conventionally this effect is reduced using a

phase locked loop (PLL) to recover the clock. PLLs work by continuously comparing the incoming clock with the regenerated clock using a long time constant, with the result that short-term fluctuations in clock frequency are attenuated. This method is analogous to fitting a flywheel to a car engine to smooth out fluctuations in crankshaft speed caused by the sequential firing of the cylinders. Using two PLLs in series can attenuate the clock frequency variations still further.

A superior method of clock recovery has been developed for the Naim DAC. It does not use one or more PLLs for clock regeneration: instead it uses 10 selectable fixed clocks. This clocking method is described in more detail in the next section.

## Naim DAC architecture



Block diagram of the Naim DAC

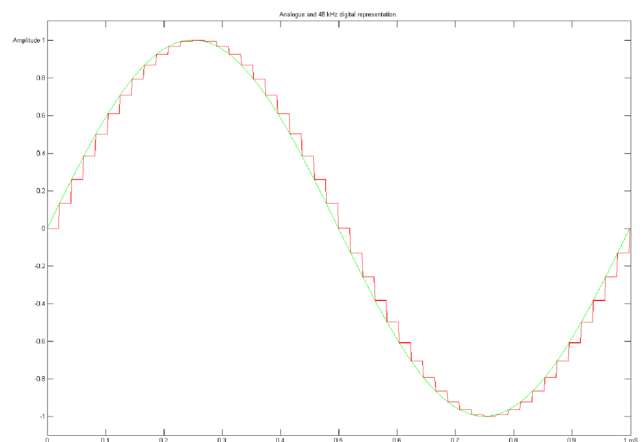
### RAM buffer jitter removal

Naim's buffer or memory method of jitter removal relies on a simple concept: the audio data is clocked into the memory at the incoming, inconsistently timed rate and is then clocked out of the memory and into the DAC chips using a precise clock. The rate at which the memory fills and empties is controlled by selecting the master clock that best matches the average incoming clock frequency. In this way the data entering the DAC chips is completely isolated from the incoming jitter. Only in rare cases will none of the Naim DAC's selectable master clocks be closely enough matched to the incoming data rate. To cope with this eventuality we have also implemented, as a backup, an asynchronous sample rate converter (ASRC).

### Oversampling and analogue filtering

When an analogue signal is converted to digital form it is no longer continuously variable; it is now a discrete representation of the original. This means that the signal amplitude is only known at certain, regularly spaced discrete time intervals determined by the sample rate. For CD the sampling rate is 44.1kHz (44,100 samples per second) and therefore the time interval between each sample is 22.7µs (microseconds). To recreate the analogue signal, the DAC holds each sample value until

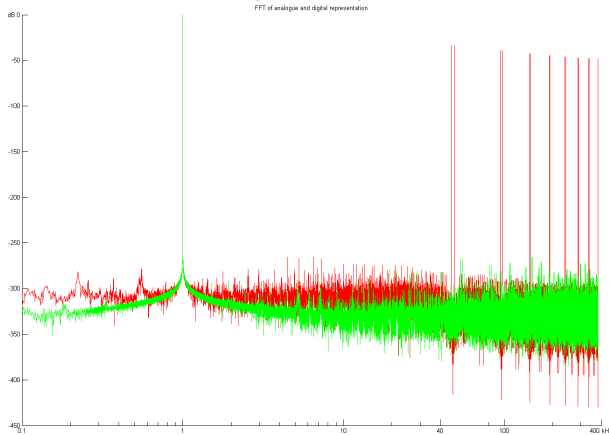
the next arrives, resulting in a staircase waveform rather than the smooth, continuous original. An example is shown below.



1kHz sine wave (green trace) and the staircase equivalent generated by a DAC chip (red trace). Sample rate is 48kHz

Looking at the staircase signal in the analogue time domain, as above, it may not look too bad. But if we look instead at the frequency spectrum of this signal (below) we see that instead of containing just the single frequency of the original analogue signal, the staircase waveform contains a lot more due to its sharp high frequency steps.

Spectral analysis of the original signal (green trace) and the unprocessed DAC output (red trace).



Note that the peak in the green trace at 1kHz overlays an equivalent peak in the red trace

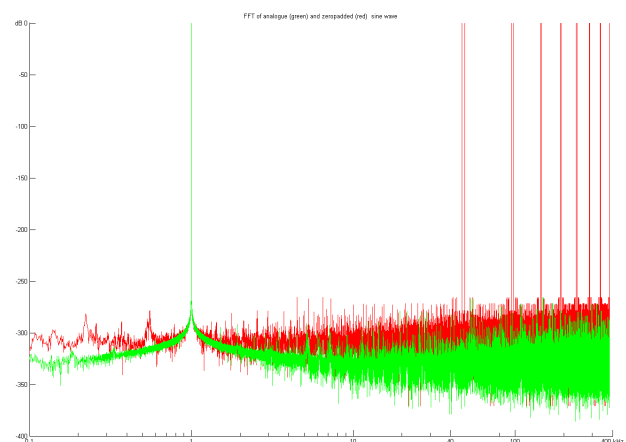
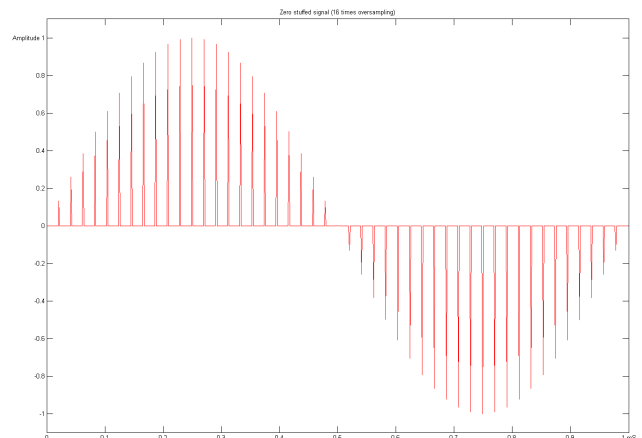
If the analogue signal is a 1kHz sine wave, as above, then the frequency spectrum of the staircase equivalent will also display a peak at 1kHz. But it additionally has peaks at every multiple of the sample rate plus or minus 1kHz (ie 47 and 49kHz, 95 and 97kHz, 143 and 145kHz, etc). In order for the DAC output to be as close as possible to the analogue original, these extra frequency components have to be removed by filtering out everything above half the sample rate. Then only those frequency components that were present in the original signal are left.

This requires a very steep low-pass filter. Achieving adequate performance using an analogue filter is extremely difficult. It requires the use of costly, high-precision components, and even then the filter performance may change with temperature, loading, etc. One way of relaxing the constraints on the analogue filter is to increase the frequency space between the audible band (up to 22.05kHz at 44.1kHz sample rate) and the first of the unwanted frequency components. One popular method of achieving this is called oversampling and is described below. By oversampling we can use a relatively simple analogue filter to remove the remaining high frequency components that the DAC introduces.

To increase the sample rate we have to insert additional samples between the original samples. If we want to double the sample rate then we need to insert one extra sample between each two original samples, if we want to quadruple the sample rate then we need to insert three extra samples between each two original samples, and so on. But what sample values do we put there? If we oversample by a factor of two we could perform linear interpolation, so that each additional sample has

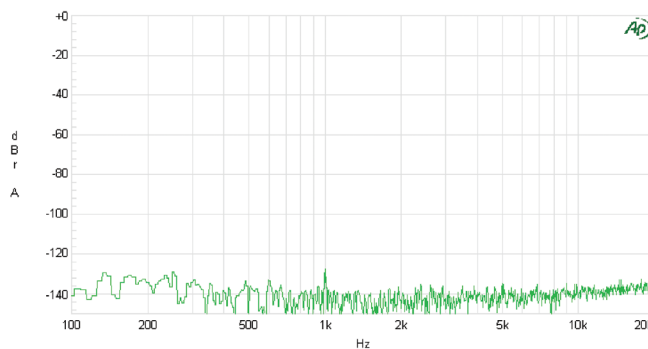
a value half way between that of the original samples on either side – but that simplistic approach will create a lot of unwanted frequency components. In fact, linear interpolation is just a very basic low-pass filter. We can do better than that!

Fortunately there is a better way of generating the new samples. First we ‘zero stuff’ the digital signals – in other words, insert the required extra samples but give them all a value of zero. When we do the result is a waveform and spectrum like that shown below. Note that the spectrum is very similar to that shown previously but all the out-of-band peaks are now of the same height as the in-band peak (0dB). If we can remove all the extra tones (above 24 kHz in the example below) then we will create a DAC output signal that has smaller steps – provided, of course, that the DAC supports the new higher sample rate. That in turn means that the remaining unwanted frequency components will be higher in frequency, allowing them to be removed using a simpler low-pass analogue filter.

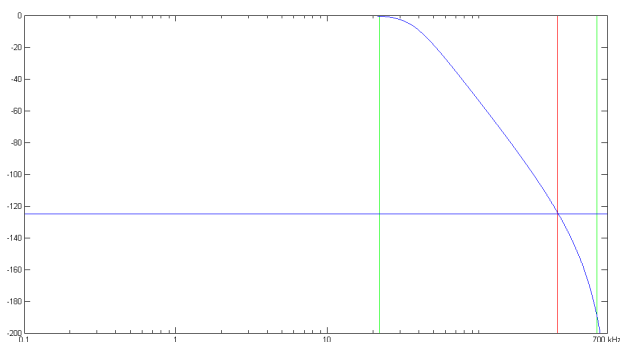


The same 1kHz signal as before (upper) and its spectrum (lower), sampled originally at 48kHz but now zero-stuffed with 15 zero-valued samples between each adjacent pair of original samples. The sample rate is now  $(16 \times 48 =) 768\text{kHz}$

Here we have oversampled the data 16 times: why not 8, 10 or any other convenient multiple? The 6th-order analogue filter used in the Naim DAC provides 36dB attenuation per octave. Working backwards, we see that with 8x oversampling applied to CD data the first image will appear at  $(8 \times 44.1 - 22.05 =) 330.75\text{kHz}$ . At this frequency the analogue filter (see simulation below) provides about 125dB attenuation. Given that 24-bit data has a dynamic range of about 144dB ( $20\log_{10}(2^{24})$ ), if we use only 8x oversampling we won't exploit the full potential of high-resolution music. So the Naim DAC uses 16x oversampling, where the first image frequency appears at  $(16 \times 44.1 - 22.05 =) 683.55\text{kHz}$ . At this frequency the analogue filter provides 191dB attenuation, exceeding 36dB per octave overall as a result of additional roll-off at high frequencies due to effects like loading of the output stage. The simulation result below illustrates this.



FFT spectrum analysis of the analogue output from the Naim DAC fed a 1kHz, -130dBFS tone with 24-bit resolution at 96kHz sample rate, no dither. A Blackman-Harris window is used with no FFT averaging. The -130dB peak at 1kHz demonstrates that the DSP and DAC system is resolving 24 bits



Simulated frequency response of the analogue output filter in the Naim DAC. The left vertical green line represents the top end of the passband for 44.1kHz sample rate, at 22.05kHz. The red vertical line represents the lowest image frequency for 8x oversampling, at which the filter attenuation is about 125dB. The right vertical green line represents the lowest image frequency for 16x oversampling, at which the filter attenuation is 191dB

How do we prove that our DAC performs as we expect? A simple way is to send in a digital, 24-bit, non-dithered -130dBFS sine wave, record the output with an Audio Precision test set and perform an FFT spectral analysis. This gives the result shown below. Note that we don't do any averaging for this measurement, and that the FFT length is fairly short (16,384 points at 100kHz sampling rate).

### Digital filtering using Naim algorithms

If we insert 15 zeros between each pair of input samples as the first stage of 16x oversampling, the frequency spectrum of the zero-stuffed signal will contain lots of unwanted components, as shown previously.

All the frequency content occurs above half the sample rate, ie above 22.05kHz in the case of CD, and must be removed by the digital filter. While it is fairly easy to design a digital filter that applies a high degree of attenuation to

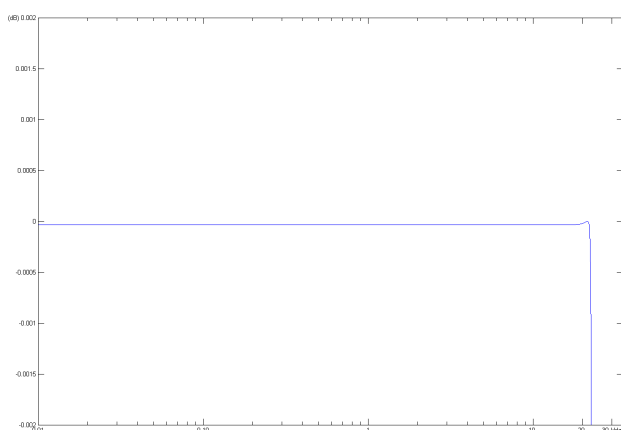
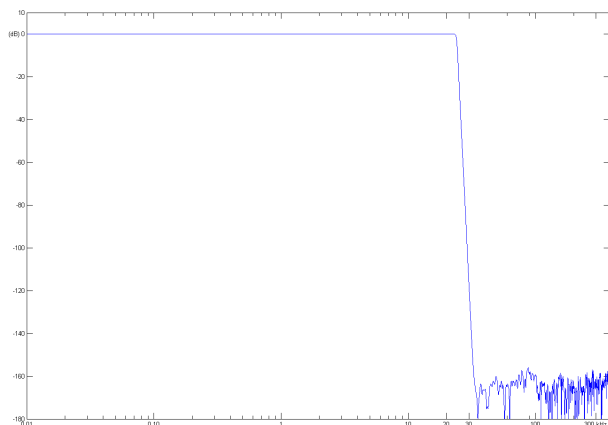
everything above 22.05kHz while having minimal effect on frequency response below 20kHz, we need to ensure that we use sufficient mathematical precision to keep the filter's arithmetic noise below -144dB at all times.

As the incoming audio can have up to 24-bit resolution, 24-bit processing will not be sufficiently accurate as it would incur rounding and/or truncation errors of the same resolution as the incoming audio. The normal solution is to use 32-bit floating point processing instead but in 32-bit IEEE floating point arithmetic the mantissa is 24 bits long, so if we have sample values close to 1 – where the exponent will be 0 – we will again achieve only 24-bit precision. (For readers unfamiliar with floating point arithmetic, numbers are represented in the basic form  $1.23456E+5$ , where the first part of the number – 1.23456 in this case – is termed the mantissa and the second part, here +5, is the exponent, ie the power of 10 by which the mantissa is multiplied. In conventional integer arithmetic  $1.23456E+5$  is written as 123,456. Note that IEEE floating point numbers use base 2 (binary) rather than base 10 representation, but the structure is the same.)

In reality it is very hard to estimate the resulting precision using floating point numbers. The best way to assess it in the context of filter designs is to use real-world signals, send them through the filter and check the outcome to see what precision was achieved. A quick test along these lines verifies that 32-bit floating point processing does not achieve the precision we require. Fortunately, more powerful processors from Analog Devices support a new type of floating point number, 40-bit floating point. Instead of having a 24-bit mantissa these use a 32-bit mantissa with 7 bits of exponent. This gives the resolution we require but keeps memory requirements fairly low (only one more byte compared to 32 bits). If we send music signals through our implementation of a filter with 40-bit floating point and analyse the results, we see that arithmetic noise is at about -156dB, which is well below the noise floor of the DAC chips.

When it comes to choosing how to implement the low-pass filter, it is all a matter of taste and how well you can implement the method you choose. Having listened to IIR (infinite impulse response) and FIR (finite impulse response) implementations of filters with identical amplitude and phase responses, we found that we prefer the IIR implementation. Even though, in a perfect world, FIR should be able to implement any IIR response to the resolution of the DACs, we found that processing loads, arithmetic noise, etc had greater influence on sound quality than the phase errors that IIR filters inherently introduce.

The chosen filter is a modified Butterworth filter to which additional poles have been added to prevent too much phase shift occurring within the audio band. The filter is implemented as efficiently as possible, using only five lines of assembly code. This ensures both low arithmetic noise (fewer additions and multiplications that cause rounding) and low power supply noise (since the DSP draws less current when it isn't calculating).



The Naim DAC digital filter response and passband ripple, input sample rate 48kHz.

## Master clock

The stability or noise of a DAC or CD player's master clock has a direct influence on the audio output. For example, if the clock frequency were to increase momentarily by 1 per cent then the analogue output frequency would increase by the same amount. So the Naim DAC's master clock has been designed to oscillate with extremely low noise. There are many types of clock frequency instability, with many different causes, but by careful design these influences can be minimised.

Phase noise is random and can be caused by internal and external influences on the clock. Power supply noise, for instance, can influence its oscillation, so in the Naim DAC the master clock has its own voltage regulator to prevent external noise influencing stability. But poor printed circuit board (PCB) layout can introduce power supply noise even when a regulator is used. The Naim DAC's PCB has six layers and is laid out such that circulating currents are kept local. All decoupling capacitors are connected with short, wide tracks to ensure low impedance and less HF noise on the power supply lines.

The Q (sharpness) of the resonant circuit also has an influence since the higher the Q, the smaller the spread of oscillation frequency. As an analogy, a bell made of bronze has a higher Q than one made of lead and so will oscillate at a more closely defined frequency (pitch). To ensure high Q, the master clock in the Naim DAC uses a high-tolerance crystal connected as a resonant tank circuit in a Colpitts configuration, with gain provided by a high impedance Field Effect Transistor (FET).

Commercially available digital audio equipment almost without exception uses Pierce oscillators instead, which are easily designed using a few passive components and one digital inverter. The digital inverter is convenient but forces the oscillation on the crystal to be a square wave rather than a natural sine wave, whereas in the Naim DAC the output from the oscillator and the signal on the crystal are sinusoidal. Once this pure oscillation is generated it is 'squared up' ready for clocking the digital circuits. This configuration has characteristically lower phase noise than a Pierce oscillator.

When the Naim DAC is playing audio from a memory stick via its USB port, the DAC is the master and its master clock runs at a fixed frequency. But when the Naim DAC is playing audio via S/PDIF, the source of the S/PDIF signal is the master and the DAC's master clock must, on average, match the frequency of the source clock. Most DACs achieve this either by using an asynchronous sample rate converter (ASRC) or a voltage-controlled crystal oscillator (VCXO).

ASRCs can work well but they rely on considerable mathematic processing, which will cause problems if not implemented very carefully. There are no ASRC chips on the market that can convert arbitrary input sample frequency to high enough frequencies that the analogue output filter can be kept fairly simple.

This means that you still have to oversample the data before the DAC, so you might as well do that properly from the outset and avoid the ASRC entirely. Moreover, since ASRC relies on averaging the incoming sample rate, not all jitter will be removed. The Naim DAC uses the built-in ASRC in the SHARC DSP only when the incoming data rate is outside the S/PDIF spec. The SHARC's ASRC has an arithmetic noise of -128dB and so it is only used in these exceptional circumstances.

VCXOs are a good solution too but since a VCXO's output frequency is controlled by a voltage, if noise is present on the control line then the VCXO's output will exhibit phase noise.

The Naim DAC approaches the problem of matching its clock frequency to the source's in a quite different way. Its master oscillator offers 10 switchable fixed frequencies which are selected so as to keep the average clock frequency the same as the source's. The SHARC DSP monitors the rate at which the RAM buffer is either filling or emptying and chooses the clock of the appropriate frequency to prevent under- or over-run of data. Unlike the VCXO solution, there is no control line to inject noise.

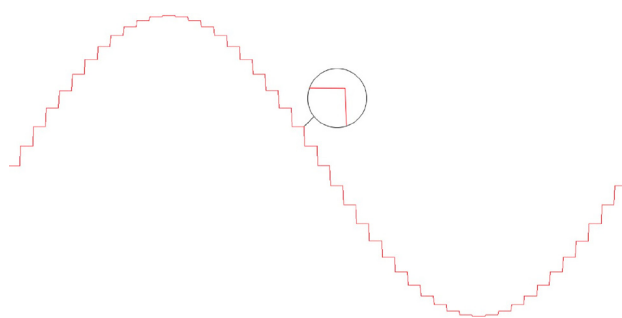
#### DAC chips

Two mono, true multi-bit Burr-Brown PCM1704K DAC chips are used in the Naim DAC – the same type as in all Naim high-end CD players including the CD555. The PCM1704K is a precision, 24-bit digital-to-analogue converter with exceptional dynamic performance whose ultra-low distortion and excellent low-level signal performance make it the ideal choice. Precision laser-trimming at the factory minimises differential linearity and gain errors, and the PCM1704K incorporates a BiCMOS sign-magnitude architecture that eliminates glitches and other nonlinearities around the zero crossing point. It is capable of running with an input data clock of 25MHz, which allows sample rates of over 700kHz.

#### Current to voltage stage (I2V)

The output signal from a true multi-bit DAC chip is a current not a voltage. But the Naim DAC's analogue outputs must carry a voltage signal, as required by the following preamplifier. So the current output of the DAC chips must be converted into an equivalent voltage signal, using a circuit called an I2V converter (because current is symbolised by the letter 'I' and voltage by the letter 'V', hence I2V).

An I2V converter must be fast, not because the audio signal itself has particularly high rate of change but because the staircase waveform from the DAC has fast edges. If the I2V converter is slow, its output will contain frequencies which were not present in the encoded audio signal. These distortions are audible and once generated cannot be removed by the analogue filter stage that follows.



Staircase DAC output with one of the fast edges magnified (16kHz sine wave at 768kHz sample rate)

The I2V converter in the Naim DAC is a Naim-designed discrete bipolar transistor stage. Each part of the circuit has been optimised for the application to achieve superior performance to a generic op-amp. The circuit was first designed on paper, based on existing knowledge. Then the design was transferred to SPICE circuit simulation software for computer analysis. This simulation allows the circuit to be tested prior to being built, and is also used to investigate the cumulative effect of component tolerances using a process called Monte Carlo analysis. SPICE speeds up the design process as it is possible to simulate hundreds of designs a week. It will not directly predict how a design will sound but it shortens the listening room testing time by weeding out circuits that do not function as well as required. Power supply, PCB layout and microphonic effects cannot be reliably modelled in SPICE but have a profound effect in the listening room.

The Naim DAC's I2V stage comprises three parts: a differential input stage, a voltage gain stage and the buffer or output stage. Overall the circuit is configured as a virtual earth amplifier, with the DAC chip's output connected to the virtual earth summing point. If the DAC chip's output terminal is subject to any voltage variation the result can be increased distortion; this circuit configuration prevents that occurring.

A differential long tail pair (LTP) is used for the input stage. This provides high input impedance, ensuring that the DAC chip's output current flows principally through the I2V stage's feedback resistor. A low impedance resistive load forces the effect of parasitic capacitance to a very high frequency, ensuring that the input stage is fast. Because the LTP transistors are biased from a constant current source and the virtual earth configuration inherently keeps them at a constant voltage, the input stage is extremely linear. If it were not it would irreversibly distort the signal.

The second, voltage gain stage is a two-transistor, cascoded common emitter arrangement with a constant current load. The first transistor provides the gain while the second provides a voltage shield for the first, so that it operates at almost constant collector-emitter voltage. This prevents the large output voltage swing from modulating the first transistor's gain characteristics (the 'Early effect') and thereby introducing distortion.



A class-A complementary push-pull emitter follower is used for the output stage. This provides low output impedance for both the feedback resistor and the following analogue filter stage.

The I2V converter's output voltage is proportional to the DAC chip's output current and the value of the feedback resistor. This makes the I2V feedback resistor a highly critical component. Both the type of resistor and how it is mounted to the PCB are tuned in the listening room.

#### Analogue output filter

Once the DAC's output signal has been converted from a current to a voltage it is time to remove the remaining unwanted frequency components using an analogue low-pass filter. The Naim DAC uses two 3rd-order (18dB per octave) filters cascaded to give a 6th-order (36dB per octave) roll-off overall. Each stage uses a Sallen and Key type filter. The buffer block uses a Naim-designed zero-feedback complementary buffer that provides high input impedance, low output impedance and is ultra-fast. Using an op-amp as a buffer can achieve good results but, because the effectiveness of the negative feedback reduces as frequency rises, op-amp performance starts to deteriorate at high audio frequencies. In active filters, this deterioration can be exacerbated as a result of the feedback capacitors demanding increasing current.

The Naim buffer operates without feedback and so its performance is consistent over a wide bandwidth, with and without load. It is configured as a true complementary, bootstrap cascaded, two-stage class-A follower. Biasing is achieved using complementary constant current sources connected to complementary inverted emitter followers which drive and bias the output followers. This connection method ensures that the biasing for the entire buffer remains constant over a wide range of operating temperature.

As with the I2V converter, Early effect distortions are substantially reduced in the first followers by means of cascode loading. The followers run at near constant current and voltage, hence they generate very low levels of distortion. Similar conditions apply to the output devices as their collectors are also isolated from the power supply via cascode transistors which are driven by the output of the first followers.

Although a Sallen-Key filter configuration is used, the filter capacitors are driven from the emitters of the output devices, not from the output itself. This connection provides a lower impedance drive and ensures tightly controlled filter roll-off to very high frequencies.

#### DSP to analogue electrical isolation

To prevent interference from the high-speed DSP engine affecting the high-resolution DAC and analogue circuits, electrical isolation must be incorporated between the two.

Digital audio must still be transferred from the DSP to the DAC and the master clock must be transferred to the DSP. To perform isolated bi-directional data transfer, the Naim DAC uses Analog Devices ADuM couplers incorporating iCoupler® technology. These are comfortably fast enough to handle the required data rates.

#### Low noise power supply

Reducing power supply (PSU) noise has long been part of Naim's design philosophy. To increase perceived and measured dynamic range, PSU noise in the Naim DAC has been reduced to an extremely low level.

The PSU begins with a custom-designed toroidal transformer. Toroidal transformers have very low magnetic leakage, which ensures that electromagnetically induced mains noise is low. The transformer has three isolated windings, feeding three sets of rectifiers and reservoir capacitors: one for the DSP, one for the clock circuits and the last for the DAC chips, I2V converters and analogue filters. The reservoir capacitors are larger than those typically used to reduce the unregulated voltage noise and provide increased short-term current capability. The three separate PSUs form part of the electrical isolation of the DSP section from the DAC chips and analogue circuits.

Low noise LM317/337 regulators smooth the unregulated voltage from the reservoir capacitors. Voltage supply to the analogue circuits is subject to further noise reduction by twelve emitter follower regulators, two for each analogue stage. The random and signal-correlated noise on the voltage rails is now at a comparable level to the noise within the audio signal.

When the PSU upgrade option is used with the Naim DAC, power supply separation is further increased by the use of a dedicated supply for the master clock circuits. It also provides a bigger toroidal transformer and bigger reservoir capacitors, and the DSP remains powered from the Naim DAC transformer to give even more separation from the analogue section.

#### Other sonic influences

As with all Naim designs, the influence of vibration-induced microphonic noise has been minimised in the Naim DAC. The starting point is a rigid aluminium chassis with 3mm-thick panels. Only at strategic points are the FR4 fibreglass printed circuit boards screwed to the chassis, with other parts of the PCB resting on pillars to reduce energy transfer. To isolate vibrations associated with reservoir capacitor charging, the power supply PCB is separate from the main PCB. Analogue stage filter capacitors that work in the audible band are prone to microphony, so susceptible components are mounted to minimise this effect.

PCB design for a DAC circuit is as critical to performance as it is for a high-end power amplifier. There are high-speed DSPs, high-resolution digital circuits and low noise analogue circuits present, all of which require different design approaches. In the Naim DAC the DSPs are placed well within the boundaries of a six-layer PCB. Multiple power pins are decoupled using multiple decoupling capacitors mounted on the bottom of the board, and the DSP also relies on inter-plane capacitance to provide low inductance decoupling. External peripheral devices such as the SDRAM are placed as close as possible to the DSP ports to minimise the loop area of high speed circulating currents. All high speed traces are measured and resistively damped accordingly to ensure that digital signal edges are not subject to ringing. Ringing radiates high frequency electromagnetic energy that could otherwise affect the analogue circuits.

The master clock drivers and timing gate are decoupled differently to slow-speed PCB design. For best performance the decoupling capacitors are placed topside to avoid using the inductive PCB vias. Decoupling traces dominate the topside, being as wide and short as possible since every millimetre of PCB trace length has a significant effect when clock signals are at 24MHz with nanosecond rise times. All high frequency traces are sandwiched on the central layers of the PCB where they are shielded by the ground and power planes that create the high frequency return current paths. Outer layers are used for low frequency signal and clock decoupling.

In the analogue circuits, different techniques are required again. Here large planed areas of PCB are detrimental to sound quality and are replaced with the star ground techniques that can be found in all Naim analogue products.

## Connectivity

- CD, DVD player – connect via S/PDIF (watch out for the switch mode power supplies of cheap digital players and the quality of S/PDIF, which may suffer RF noise)
- PC – use an external USB sound card with a lossless driver, eg ASIO
- MacBook or Mac mini – use the computer's S/PDIF optical connection
- Set-top box – connect via S/PDIF optical and set the set-top box to PCB
- iPod/iPhone give bit-perfect playback with data from properly ripped CDs
- UPNP: iPod touch/iPhone – lossless files played using PlugPlayer are bit-perfect
- USB memory stick – Naim DAC will play WAV files with sample rates of up to 768kHz (although some USB sticks may be too slow to deliver audio at high sample rates - 768kHz audio requires up to 6.1 Mbytes per second constant data flow)
- Remote control – via wired, IR and Apple remote (transcodes to standard RC5 for volume)

### Note:

Some UPNP servers are not bit perfect. Windows Media Player 11 has been tested and produces good results with the Naim DAC, as does the iPod/iPhone running PlugPlayer.

### MS Windows PC

We have successfully used an M-Audio Transit USB external sound card – but be sure to install the latest drivers from the M-Audio website and to use only one audio player at a time. For best quality from ripped 44.1kHz audio, set the Transit to 'in and out'; if it is set to 'out only' it will upsample to 88.2kHz.

### Google Android phone (currently under development)

Install BK Mobility's free MountUSB app, transfer music files to the phone's SD card, plug into the Naim DAC and control in the same way as a USB memory stick.

# Some of the possibilities .....

## Naim CD5XS



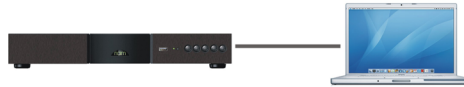
Connect via S/PDIF

## HDX



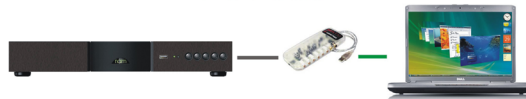
Connect via S/PDIF

## MAC audio



Connect via S/PDIF  
Can control via Wi-Fi  
using Apple remote app

## PC Audio



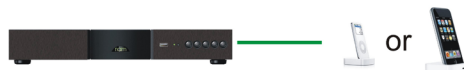
Connect S/PDIF via a  
bit transparent sound card  
Can control via iPhone  
using UPnP or VNC

## Game and TV



Connect via S/PDIF  
Can connect via  
optical to prevent  
AV ground loops

## iPod Audio



Connect via  
iPod USB cable

## iPod Audio +



Connect iPod  
(or iPhone or iTouch) via  
USB cable and stream  
via Wi-Fi from UPnP NAS  
or internet radio app  
Control from another iTouch

## Memory stick Audio



Plug 'n' Play

## FAQs

- Why is there no USB input for streaming audio from a computer?  
This would entail an electrical connection to a noisy electrical environment making all inputs sound worse. Using an external USB sound card connected to the Naim DAC via optical S/PDIF gives better results. (For example, the M-Audio Transit – it's powered from USB.) Or you can use the optical output direct from the computer if it has one. A FireWire connection is not included for the same reason.
- Why S/PDIF optical rather than coaxial?  
Coax can sound better but optical has the advantage that it prevents ground loops and isolates the ground system of the source, which may be noisy, from that of the Naim DAC.
- Why is there no balanced digital input?  
Naim DAC is designed for the domestic environment where balanced digital connections are rarely used. While the balanced interface is good for long digital runs from, say, studio to mixing desk, it exacerbates the RF noise problem because its operating voltage is higher.
- Who is the target customer?  
People who appreciate good sound quality and have a quality digital source that they would like to upgrade. If they have a variety of digital sources then the Naim DAC is even better value for money.
- What does 'bit perfect' mean?  
What digital data goes in, comes out – exactly.
- What is jitter exactly?  
Jitter is variations in the time separation of digital audio samples. All S/PDIF induced jitter coming in to the Naim DAC is removed, except for the encoded jitter caused by the mastering analogue to digital conversion done in the studio where the CD was mastered.